



09/17/2004 01:52 PM

Slater & Matsil, L.L.P. 9727329218 2/3

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IRA S. MATSIL
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Kristin R. Hayes

(Depositor's name)

KHayes

(Signature)

9/17/04

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,113	12/19/2000	Mihel Seitz	00P9102US	4212

TITLE OF INVENTION: METHOD FOR FABRICATING TRANSISTORS HAVING DAMASCENE FORMED GATE CONTACTS AND SELF-ALIGNED BORDERLESS BIT LINE CONTACTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	09/24/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, THANH Y	2827	438-243000

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2

3

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(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Infineon Technologies AG

Munich, Germany

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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Ira S. Matsil, 35,272

September 17, 2004

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Slater & Matsil, L.L.P. 9727329218 1/3

Slater & Matsil, L.L.P.

Suite 1000
17950 Preston Road
Dallas, Texas 75252-5793
Phone: 972-732-1001 Facsimile: 972-732-9218

FACSIMILE COVER SHEET

To Commissioner for Patents	Total Pages Sent: 3
Mail Stop Issue Fee	(including cover sheet)
Facsimile Number: (703) 746-4000	Transmission Date: September 17, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Seitz, *et al.* Docket No.: 00P9102US
Serial No: 09/740,113 Art Unit: 2827
Date Filed: December 19, 2000
Title: Method for Fabricating Transistors having Damascene Formed Gate Contacts and Self-Aligned Borderless Bit Line Contacts

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- Part B - Fee Transmittal (1 original and 1 copy)

Respectfully submitted,

Kristin Hayes
Legal Assistant

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